UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,194	11/20/2001	James S. Koford	01-390	3156

24319 7590 03/01/2005

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
PALADINI, ALBERT WILLIAM	
ART UNIT	**PAPER NUMBER**
2125	

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,194	KOFORD ET AL.	
	Examiner	Art Unit	
	Albert W Paladini	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-16* is/are allowed.

6)☒ Claim(s) *1-9 and 11-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/02,6/03,1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-9 and 17-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The description of figures 1 and 2 on pages 9-17 do not explain or depict a configuration described in claims 1 and 17. The EDA tools in figure 1 reside in software 104, and are part of design utility 100, as explained on page 9 of the specification. The EDA tools are not shown in figure 2.

Appropriate correction and clarification are required.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are:

Claim 1

The claim recites elements such as the "design utility", "EDA tools", "at least one dynamic template", "at least one static template", but does not recite how they are interconnected structurally or functionally, in order to perform the function recited in the preamble.

Appropriate correction and clarification are required.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

6. Claims 17-21 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01.

Claim 17

The claim does not contain steps which lead to the objective of "designing an integrated circuit" as, recited in the preamble. A design utility is accessed in the first step. A "dynamic template" is displayed in the second step. Finally "two symbols are arranged in the last step. These steps do not appear to contain a complete sequence of logical events leading to the design of an integrated circuit. It is also not clear what is meant by "the dynamic template implements at least two symbols".

Appropriate correction and clarification is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-9 and 17-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Heile (6026226).

This rejection is made to the extent that the claims are understood by considering the recited objective and the elements, which are logically consistent with the objective.

Heile discloses a system for integrated circuit design, which includes a user interface shown as block diagram 100 in figure 5, and represented as a hierarchy tree in figure 6. In figure 2, Heile discloses the use of templates in conjunction with EDA tools. Step 56 includes generating design file templates with the EDA tool for all blocks present in the top-level block diagram of step 54. After the designer has created a block, which has not yet been implemented, the system may generate a design file template. Such templates may display a block in a window format including, for example, a title, a date, etc. around the boundaries. It may also include some details of the functional content depicted within the window. The design file templates may be in any specified design format including VHDL, AHDL, Verilog, block diagram, schematic, or other like format. In the case of a VHDL block the template may also include much of the formatting and necessary syntax for any VHDL block.

Allowable Subject Matter

9. Claims 10-16 are allowed.

10. The following is a statement of reasons for the indication of allowable subject matter: None of the references cited or the art searched disclose or teach alone or in combination the system for designing an integrated circuit with the first computer

including the first design navigator, the first project coordinator, at least two EDA tools, a dynamic template, and the second computer with the corresponding elements all coupled to the network as recited in claim 10.

Relevant Prior Art

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

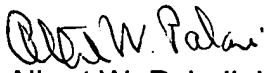
Van Dyke (5625565) discloses a system and method for generating templates for logical systems used in circuit design where the function templates module includes data representing logical pin names, logical elements, and pin-to-pin dependency notation for each function template. A symbol generation rules module includes data describing the rules to be used in building functional logic symbols (schematic symbols). The standard defines some of these rules, such as the height of dependency notation text in relation to the size of the functional logic symbol of the component. A schematic symbols module includes data representing the graphical symbols that are output to a computer monitor during EDA.

Khazei (6834380) teaches that tools for automated component placement have become commonplace in the design and fabrication of modern electronic systems and devices (such as integrated circuits). In such a tool, which translates a logical or schematic circuit description into a template for the placement of components within an actual prototype. Input data for an automated placement tool may include a functional description of logical flow or signal flow, e.g. as embodied in a SPICE (for `Simulation Program (with) Integrated Circuit Emphasis`) netlist or a hardware description language (or `HDL`) file. The tool may also receive data such as constraints on the size and/or shape of the finished prototype. When used to design integrated circuits, automated placement tools are also called `floorplanners,` although similar tools may also be used to design multichip modules (MCMs), circuit boards or subassemblies, or even complete assemblies such as end-user and consumer products.

12. Any inquiry concerning this communication or earlier communication from the examiner should be direct to Albert W. Paladini whose telephone number is (571) 272-3748. The examiner can normally be reached from 7:30 to 3:30 PM on Monday, Tuesday, Thursday, and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Leo P. Picard, can be reached on (571) 272-3749. The official fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Albert W. Paladini
Primary Examiner
Art Unit 2125

February 22, 2005